SON-1351 PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In the Divisional Application of the Patent Application of	
HIROYUKI MIWA	Group Art Unit: 2508
Serial No. Not assigned	Examiner: S. Loke
Filed: January 28, 2002	
For: METHOD OF MAKING A BIPOLAR TRANSISTOR HAVING A REDUCED BASE TRANSIT TIME (as amended)	

PRELIMINARY AMENDMENT

Commissioner for Patents
Washington, D.C. 20231

Sir:

Prior to an initial examination of the above-identified divisional patent application, please enter the following amendments.

IN THE TITLE:

Please amend the title of the invention to read -- METHOD OF MAKING A BIPOLAR TRANSISTOR HAVING A REDUCED BASE TRANSIT TIME --.

IN THE DRAWINGS:

Please note the changes to Fig. 3 in which the labels have been reversed for the curves initially designated as "BASE (p)" and "LINK BASE LAYER (p)," and the changes to Figs. 4A to 4C and 5A to 5C which are to be labeled as -- (PRIOR ART) --.

IN THE SPECIFICATION:

Please replace the paragraph beginning at page 1, line 8, with the following rewritten paragraph:

--Recently, in the field of semiconductor devices such as LSIs, there have been strong demands toward enhancement in performance of bipolar transistors. The enhancement in the performance of bipolar transistors can be achieved by the shortening of a base transit time due to shortening of a base thickness by lowering of a base resistance, and by reduction of a parasitic capacitance represented by a base-collector capacitance.--

Please replace the paragraph beginning at page 2, line 5, with the following rewritten paragraph:

--The bipolar transistor having the above-described structure is fabricated in the following procedures.

First, as shown in FIG. 4A, an insulating film (SiO_2 film) 2 having a thickness of from 100 to 200 nm is formed over the surface of a silicon substrate 1 by or CVD.

As shown in FIG. 4B, an opening is formed for a base electrode of the bipolar transistor. Reference numeral 2a indicates an opening side wall. A p-type polysilicon (poly-Si) film 3 having a thickness of from 100 to 200 mm is formed over the surface by CVD. The p-type poly-Si film 3 serves as a base electrode. It is to be noted that the doping of a p-type impurity to the poly-Si can be also performed by ion implantation.

Next, as shown in FIG. 4C, an insulating film (SiO_2 film) 4 having a thickness of from 300 to 400 nm is formed over the surface of the wafer by CVD, and then an opening 10 for forming an emitter and a base is formed by dry etching, of the laminated films, the SiO_2 film 4 and the p-type poly-Si film 3. After that, an insulating film (SiO_2 film) 5 having a thickness of from 10 to 20 nm is formed over the surface by CVD, and a p-type impurity diffusion layer 6 is formed by ion implantation through the SiO_2 film 5. In this case, for example, ions of BF_2 are implanted in a dose of from $1x10^{13}$ to $1x10^{14}$ cm^{-2} at an implantation energy of from 20 to 30 KeV. The p-type impurity diffusion layer 6 serves as the base, and the

SiO_2 film 5 having a thickness of from 10 to 20 nm serves as a buffer layer for preventing a channeling tail upon ion implantation for forming the base. The ion implantation is followed by heat-treatment (annealing) for 10 to 20 minutes at 900°C, to form a P^+ contact layer (graft contact) 3a in the silicon substate 1 by diffusion from the p-type poly-Si film 3.

Next, as shown in FIG. A, a side wall forming insulating film (SiO_2 film) 7 having a thickness of from 400 to 600 nm is formed over the surface by CVD. The SiO_2 film 7 is then removed by anisotropic etching such as RIE so as to form side walls 7a made of the SiO_2 film in the opening for forming an emitter and a base, as shown in FIG. 5B. The side wall 7a has a function of isolating the base electrode made of the p-type poly-Si film 3 from an emitter electrode which will be formed later.--

Please replace the paragraph beginning at page 4, line 14, with the following rewritten paragraph:

--In the bipolar transistor having the above-described base-emitter structure, the concentration of the base 6 at a portion directly under the emitter 9 is high, and thereby an emitter-base withstand voltage is

determined at this portion, thus obtaining only a withstand voltage from 2 to 4 V.

To apply such a bipolar transistor to TTLI/0 or the like, an emitter-base withstand voltage of about 3.5 V or more is required. Therefore, in general, the emitter-base withstand voltage is required to be ensured by increasing an ion implantation energy upon formation of the base 6 (see Fig. 4C) for reducing an impurity concentration of the base at the emitter-base junction. --

Please replace the paragraph beginning at page 6, line 1, with the following rewritten paragraph:

--A semiconducting substrate; a first impurity diffusion layer having a first conducting type, which is formed in the semiconducting substrate; --

Please replace the paragraph beginning at page 14, line 7, with the following rewritten paragraph:

-- FIGs. 1A, 1B and FIGs. 2A, 2B are process diagrams illustrating a method of fabricating a bipolar transistor of the present invention. These figures are sectional views showing the upper side of a substrate, particularly,

an emitter portion and a base portion of an npn-transistor.

First, like the prior art method shown in FIGs. 4A and 4B, a SiO_2 film 2 (thickness: 100 to 200 nm) having opening side walls 2a and a p-type poly-Si film 3 (thickness: 100 to 200 nm) are formed on a silicon substrate 1 as a semiconducting substrate. Then, as shown in FIG. 1A, a SiO_2 film 4 having a thickness of from 300 to 400 nm is formed on the poly-Si film 3 by CVD. Then, an opening 10 for forming an emitter and a base is formed by etching (RIE) of the SiO_2 film 4 and the poly-Si film 3. A SiO_2 film 5 having a thickness of from 10 to 20 nm is formed over the surface by CVD, and then a p-type impurity diffusion layer 11 is formed by ion implantation under a condition specified by the present invention. The p-type impurity diffusion layer 11 serves as a link base layer. It is to be noted that the thin SiO_2 film 5 serves a buffer layer for preventing the channeling tail upon ion implantation for forming the link base layer. --

Please replace the paragraph beginning at page 15, line 9, with the following rewritten paragraph:

--The ion implantation condition for forming the p-type impurity diffusion layer (link base layer) 11 is as follows:

implanted ion: BF_2

energy: 5-20 KeV

dose: $1x10^{12}$ - $1x10^{14}$ cm^{-2}

diffusion depth of link base layer: 30 to 50 nm. --

Please replace the paragraph beginning at page 15, line 13, with the following rewritten paragraph:

--The ion implantation of BF_2 at a low energy of from 5 to 20 KeV is equivalent to the ion implantation of B (boron) at a low energy of from 1 to 5 KeV. --

Please replace the paragraph beginning at page 15, line 21, with the following rewritten paragraph:

--After the link base layer 11 is formed by ion implantation of BF_2, as shown in FIG. 1B, ions of a p-type impurity such as boron (B) are implanted in a dose of from $1X10^{12}$ to $1x10^{14}$ cm^{-2} at an energy of from 10 to 100KeV, to form a base 12 as a p-type impurity diffusion layer. --

Please replace the paragraph beginning at page 16, line 9, with the following rewritten paragraph:

--With the above-described sequential processes, (1) the concentration of the base 12 (including the link base layer 11) at a portion directly under the side wall 7a isolates the emitter from the base without any increase in the base concentration at a portion directly under the emitter, thus preventing variations in characteristics due to variations in a correct current or the base re-recombination current at such a portion, and ensuring reliability; and (2) an increase in the thickness of the base 12 is suppressed. --

Please replace the paragraph beginning at page 16, line 19, with the following rewritten paragraph:

--After that, as shown in FIG. 2A, heat-treatment (annealing) is performed for 10 to 20 minutes at 900°C, to diffuse the p-type impurity from the p-type poly-Si film 3 to the Si substrate, thus forming a P^+ contact layer 3a. The p^+ contact layer 3a serves as a graft base. In addition, the heat-treatment may be shared with the heat-treatment for emitter diffusion which will be performed

later. Thus, the shallow diffusion for the link base layer and the base can be achieved. A side wall forming SiO_2 film having a thickness of from 400 to 600 nm is formed over the surface. After that, the SiO_2 film is removed by anisotropic etching such as RIE so as to form side walls 7a made of the SiO_2 film. The side wall 7a has a function of isolating the base electrode from an emitter electrode which will be formed later. --

Please replace the paragraph beginning at page 18, line 19, with the following rewritten paragraph:

--As shown in the figure, the diffusion depth of the link base layer 11 is equal to or less than that of the emitter 9, and the concentration of the link base layer 11 is equal to or more than that of the base 12. --

IN THE ABSTRACT:

Please replace the Abstract with the following:

A bipolar transistor has a high performance and high reliability, which are obtained by enhancing a withstanding voltage between an emitter and a base. The bipolar transistor includes a first impurity diffusion layer in a semiconducting substrate, an opening disposed in the first conductive film. A third impurity diffusion

layer is formed so as to contain the second diffusion layer and side walls are formed on the side walls of the opening. A fourth impurity diffusion layer in the third impurity diffusion layer is formed in the opening surrounded by the side walls.

IN THE CLAIMS:

Please cancel claims 1 to 6 without prejudice or disclaimer.

Please retain claims 7-8, without change, amend claim 9 and add claims 10-15. Claims 7-15 are presented here for the convenience of the Examiner.

7. (unamended) A method of fabricating a bipolar transistor comprising the steps of:

forming on a semiconducting substrate a first insulating film having a pattern in which the surface of the semiconducting substrate is partially exposed from said first insulating film;

sequentially forming a first conductive film and a second insulating film over the surface of said

semiconducting substrate formed with said first insulating film, and then forming an opening portion so as to expose the surface of said semiconducting substrate;

forming a third insulating film on said opening portion and said conductive film;

forming a first impurity diffusion layer having a first conducting type by applying ion implantation to said semiconducting substrate at a first energy through said third insulating film;

forming a second impurity diffusion layer having the first conducting type by applying ion implantation to said semiconduting substrate at a second energy;

forming a third impurity diffusion layer having the first conducting type in said semiconducting substrate connected to said first conductive layer;

forming side walls made of a fourth insulating layer on side walls of said opening portion of said semiconducting substrate in which said first, second and third impurity diffusion are formed;

forming a second conductive film in said opening portion so as to be connected to said first impurity diffusion layer; and

forming a fourth impurity diffusion layer having a second conducting type in said second impurity diffusion

layer by ion implantation applied through said second conductive layer.

8. (unamended) A method of fabricating a bipolar transistor according to claim 7, wherein said second impurity diffusion layer is formed by ion implantation at said second energy, and thereafter a fifth impurity diffusion layer is formed under said first impurity diffusion layer by ion implantation at a third energy.

Please amend claim 9 as follows:

9. (once amended) A method of fabricating a bipolar transistor according to claim 7, wherein said first energy is lower than said second energy.

Please add the following new claims:

10. (new) A method of fabricating a bipolar transistor comprising:

forming a graft base layer from a first impurity diffusion layer created by ion implantation, wherein said graft base layer is of a first conducting type and is formed in a semiconductor substrate;

forming a first conductive film on said semiconductor substrate which is connected to said graft base layer;

forming an opening in said first conductive film;

forming a link base layer from a second impurity diffusion layer created by ion implantation, wherein said link base layer is of the first conducting type, is formed in a portion of said semiconductor substrate which is exposed by said opening portion, and is connected to said graft base layer;

forming a base layer from a third impurity diffusion layer, wherein said base layer is of the first conducting type, is formed in said semiconductor substrate, and is formed to contain said link base layer;

forming side walls in said opening portion from an insulating film, said side walls defining a central aperture; and

forming an emitter from a fourth impurity diffusion layer created by ion implantation, wherein said emitter is of a second conducting type, is formed in a portion of said semiconducting substrate exposed by said central aperture, is surrounded by said side walls, and is formed in said base layer;

wherein said link base layer has a diffusion depth equal to or less than a diffusion depth of said emitter layer.

11. (new) A method as claimed in claim 10, further comprising forming a collector from a fifth impurity diffusion layer, wherein said collector is of the second conducting type, is formed directly under said link base layer and has a maximum impurity concentration with a diffusion depth deeper than a diffusion depth for a maximum impurity concentration of said base layer.

12. (new) A method as claimed in claim 11, further comprising reducing an impurity concentration in a lower portion of said base layer with said collector layer.

13. (new) A method as claimed in claim 11, further comprising forming said graft base layer with a gap therein aligned with the opening in the first conductive film.

14. (new) A method as claimed in claim 11, wherein said forming a link base layer further comprises forming

said link bas layer on opposite sides of the emitter layer.

15. (new) The method as claimed in claim 11, wherein said forming a link base layer further comprises forming said link base layer with a depth of about 30 nm to 50 nm.

REMARKS

The foregoing amendments are made prior to the initial examination of the above-identified divisional application. Examination in light of these amendments is respectfully requested. This present application is a divisional of parent application Serial No. 08/932,832 which is also a continuation of parent application Serial No. 08/532,057. If the Examiner has any suggestions for placing the present application in even better form, the Examiner is invited to telephone the undersigned.

Dated: January 28, 2002 By:

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Appendix

IN THE TITLE:

Please amend the title of the invention to read -- METHOD OF MAKING A BIPOLAR TRANSISTOR [AND METHOD OF FABRICATING THE SAME] HAVING A REDUCED BASE TRANSIT TIME --

IN THE SPECIFICATION:

Please replace the paragraph beginning at page 1, line 8, with the following rewritten paragraph:

--Recently, in the field of semiconductor devices such as LSIs, there have been strong demands toward enhancement in performance of bipolar transistors. The enhancement in the performance of bipolar transistors can be achieved by the shortening of a base transit time due to shortening of a base thickness[,] by lowering of a base resistance, and by reduction of a parasitic capacitance represented by a base-collector capacitance.--

Please replace the paragraph beginning at page 2, line 5, with the following rewritten paragraph:

--The bipolar transistor having the above-described structure is fabricated in the following procedures. First, as shown in FIG. 4A, an insulating film (SiO_2 film)

2 having a thickness of from 100 to 200 nm is formed over the surface of a silicon substrate 1 by [CVD (Chemical Vapor-phase Deposition) or CVD.

As shown in FIG. 4B, an opening is formed for [forming] a base electrode of the bipolar transistor [is formed]. Reference numeral 2a indicates an opening side wall. A p-type polysilicon (poly-Si) film 3 having a thickness of from 100 to 200 mm is formed over the surface by CVD. The p-type poly-Si film 3 serves as a base electrode. It is to be noted that the doping of a p-type impurity to the poly-Si can be also performed by ion implantation.

Next, as shown in FIG. 4C, an insulating film (SiO_2 film) 4 having a thickness of from 300 to 400 nm is formed over the surface of the wafer by CVD, and then an opening 10 for forming an emitter and a base is formed by dry etching, [(for example, RIE)] of the laminated films, the SiO_2 film 4 and the p-type poly-Si film 3. After that, an insulating film (SiO_2 film) 5 having a thickness of from 10 to 20 nm is formed over the surface by CVD, and a p-type impurity diffusion layer 6 is formed by ion implantation through the SiO_2 film 5. In this case, for example, ions of [BF^2] BF_2 are implanted in a dose of from $1x10^{13}$ to $1x10^{14}$ cm^{-2} at an implantation energy of from 20

to 30 KeV. The p-type impurity diffusion layer 6 serves as the base, and the SiO_2 film 5 having a thickness of from 10 to 20 nm serves as a buffer layer for preventing a channeling tail upon ion implantation for forming the base. The ion implantation is followed by heat-treatment (annealing) for 10 to 20 minutes at 900°C, to form a P^+ contact layer (graft contact) 3a in the silicon substate 1 by diffusion from the p-type poly-Si film 3.

Next, as shown in FIG. A, a side wall forming insulating film (SiO_2 film) 7 having a thickness of from 400 to 600 nm is formed over the surface by CVD. The SiO_2 film 7 is then removed by anisotropic etching such as RIE so as to form side walls 7a made of the SiO_2 film in the opening for forming an emitter and a base, as shown in [() FIG. 5B[)]. The side wall 7a has a function of isolating the base electrode made of the p-type poly-Si film 3 from an emitter electrode which will be formed later.--

Please replace the paragraph beginning at page 4, line 14, with the following rewritten paragraph:

--[Incidentally, in] In the bipolar transistor having the above-described base-emitter structure, the concentration of the base 6 at a portion directly under

the emitter 9 is high, and thereby an emitter-base withstand voltage is determined at this portion, thus obtaining only a withstand voltage from 2 to 4 V.

To apply such a bipolar transistor to TTLI/0 [(Transistor-Transistor Logic Circuit Input/Output)] or the like, an emitter-base withstand voltage of about 3.5 V or more is required. Therefore, in general, the emitter-base withstand voltage is required to be ensured by increasing an ion implantation energy upon formation of the base 6 (see Fig. 4C) for reducing an impurity concentration of the base at the emitter-base junction. --

Please replace the paragraph beginning at page 6, line 1, with the following rewritten paragraph:

--[A bipolar transistor comprising: a]

A semiconducting substrate[:]; a first impurity diffusion layer having a first conducting type, which is formed in the semiconducting substrate; --

Please replace the paragraph beginning at page 14, line 7, with the following rewritten paragraph:

-- FIGs. 1A, 1B[A] and FIGs. 2A, 2B are process diagrams illustrating a method of fabricating a bipolar transistor of the present invention. These figures are sectional views showing the upper side of a substrate, particularly, an emitter portion and a base portion of an npn-transistor.

First, like the prior art method shown in FIGs. 4A and 4B, a SiO_2 film 2 (thickness: 100 to 200 nm) having opening side walls 2a and a p-type poly-Si film 3 (thickness: 100 to 200 nm) are formed on a silicon substrate 1 as a semiconducting substrate. Then, as shown in FIG. 1A, a SiO_2 film 4 having a thickness of from 300 to 400 nm is formed on the poly-Si film 3 by CVD. Then, an opening 10 for forming an emitter and a base is formed by etching (RIE) of the SiO_2 film 4 and the poly-Si film 3. A SiO_2 film 5 having a thickness of from 10 to 20 nm is formed over the surface by CVD, and then a p-type impurity diffusion layer 11 is formed by ion implantation under a condition specified by the present invention. The p-type impurity diffusion layer 11 serves as a link base layer. It is to be noted that the thin SiO_2 film 5 serves a buffer layer for preventing the channeling tail upon ion implantation for forming the link base layer. --

Please replace the paragraph beginning at page 15, line 9, with the following rewritten paragraph:

--The ion implantation condition for forming the p-type impurity diffusion layer (link base layer) 11 is as follows:

implanted ion: $BF_2[F^2]$

energy: 5-20 KeV

dose: $1x10^{12}$ - $1x10^{14}$ cm^{-2}

diffusion depth of link base layer: 30 to 50 nm. --

Please replace the paragraph beginning at page 15, line 13, with the following rewritten paragraph:

--The ion implantation of $BF_2[F^2]$ at a low energy of from 5 to 20 KeV is equivalent to the ion implantation of B (boron) at a low energy of from 1 to 5 KeV. --

Please replace the paragraph beginning at page 15, line 21, with the following rewritten paragraph:

--After the link base layer 11 is formed by ion implantation of $BF_2[F^2]$, as shown in FIG. 1B, ions of a p-type impurity such as boron (B) are implanted in a dose of

from $1X10^{12}$ to $1x10^{14}$ cm^{-2} at an energy of from 10 to 100KeV, to form a base 12 as a p-type impurity diffusion layer. --

Please replace the paragraph beginning at page 16, line 9, with the following rewritten paragraph:

--With the above-described sequential processes, (1) the concentration of the base 12 (including the link base layer 11) at a portion directly under the side wall 7a [for] isolates [isolating] the emitter from the base without any increase in the base concentration at a portion directly under the emitter, thus preventing variations in characteristics due to variations in a correct current or the base re-recombination current at such a portion, and ensuring reliability; and (2) an increase in the thickness of the base 12 is suppressed. --

Please replace the paragraph beginning at page 16, line 19, with the following rewritten paragraph:

--After that, as shown in FIG. 2A, heat-treatment (annealing) is performed for 10 to 20 minutes at 900°C, to diffuse the p-type impurity from the p-type poly-Si film 3 to the Si substrate, thus forming a P^+ contact layer 3a.

The p^+ contact layer 3a serves as a graft base. In addition, the heat-treatment may be shared with the heat-treatment for emitter diffusion which will be performed later. Thus, the shallow diffusion for the link base layer and the base can be achieved. [As shown in FIG. 1B, a] A side wall forming SiO_2 film having a thickness of from 400 to 600 nm is formed over the surface. After that, the SiO_2 film is removed by anisotropic etching such as RIE so as to form side walls 7a made of the SiO_2 film. The side wall 7a has a function of isolating the base electrode from an emitter electrode which will be formed later. --

Please replace the paragraph beginning at page 18, line 19, with the following rewritten paragraph:

--As shown in the figure, the diffusion depth of the link base layer 11 is equal to or less than that of the emitter 9, and the [surface] concentration of the link base layer 11 is equal to or more than that of the base 12 -

IN THE ABSTRACT:

Please replace the Abstract with the following:

A bipolar transistor [with] has a high performance and high reliability, which [is] are obtained by enhancing a

withstanding voltage between an emitter and a base; [and a method of fabricating the same]. The bipolar transistor includes a first impurity diffusion layer in a semiconducting substrate[;], an opening disposed in the first conductive [layer; a] film. A third impurity diffusion layer is formed so as to contain the second diffusion layer[;] and side walls are formed on the side walls of the opening. [;and a] A fourth impurity diffusion layer in the third impurity diffusion layer is formed in the opening surrounded by the side walls.

APPENDIX

CLAIM AMENDMENT

IN THE CLAIMS:

9. (once amended) A method of fabricating a bipolar transistor according to claim 7, wherein said first energy is lower than said second energy.

FIG. 3

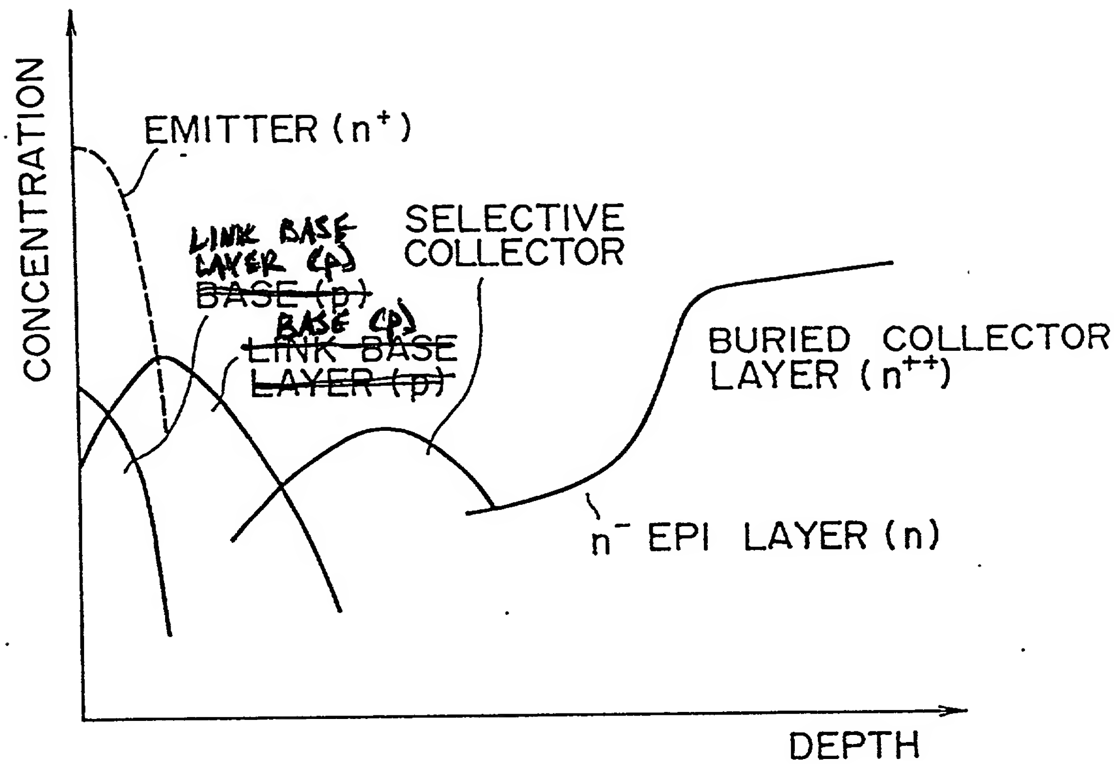
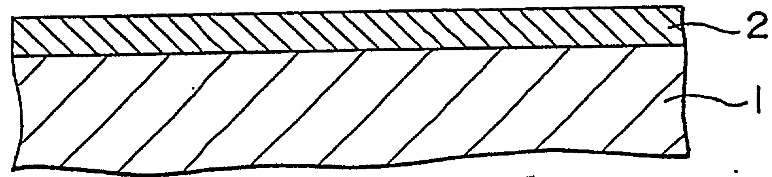
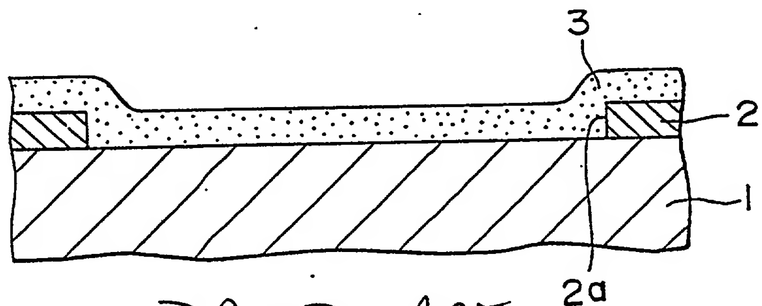

CONCENTRATION
EMITTER (n^+)
LINK BASE LAYER (p)
BASE (p)
SELECTIVE COLLECTOR
BURIED COLLECTOR LAYER (n^{++})
n^- EPI LAYER (n)
DEPTH

FIG. 4A



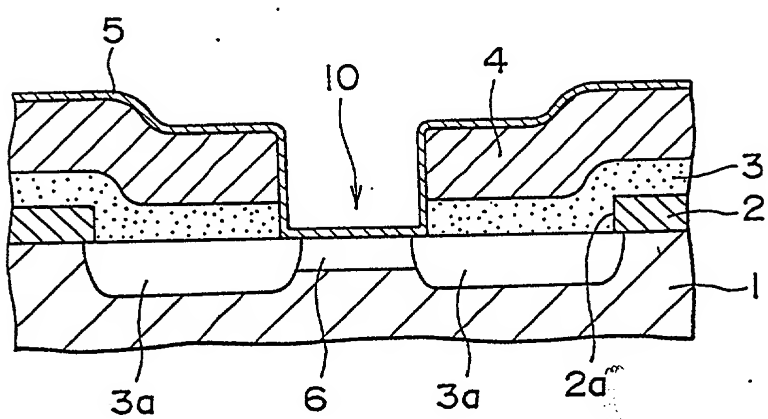
PRIOR ART

FIG. 4B



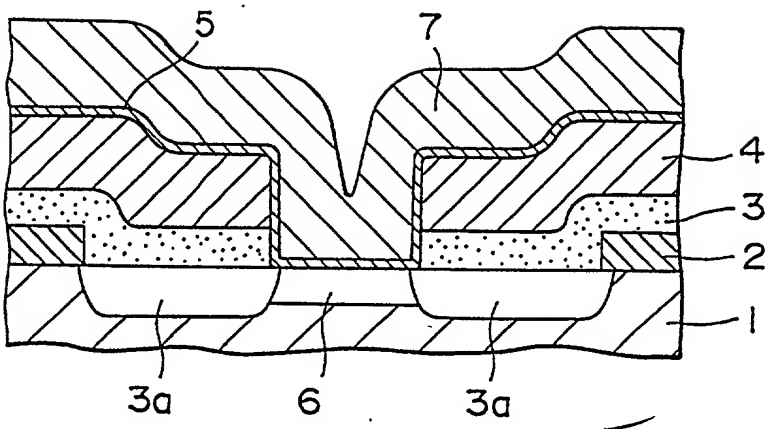
PRIOR ART

FIG. 4C



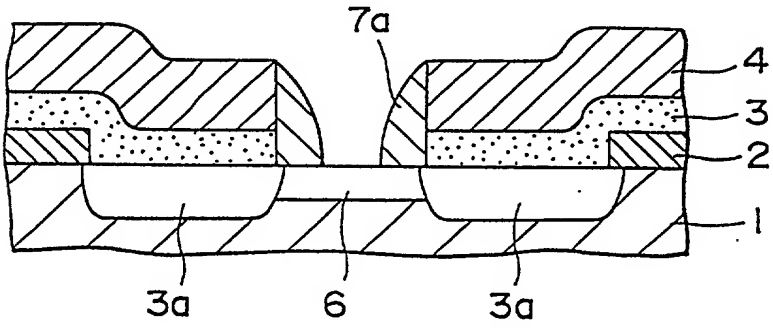
PRIOR ART

FIG. 5A



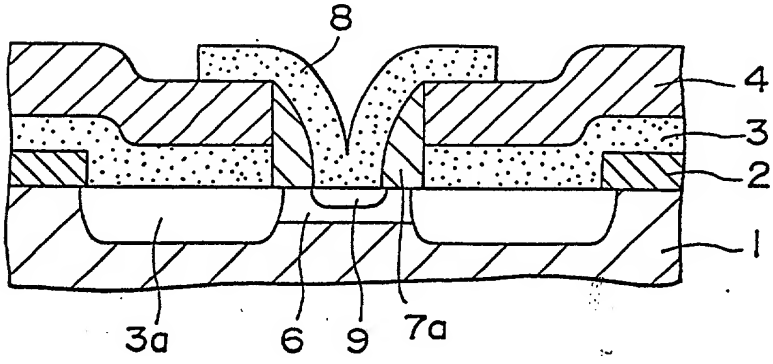
PRIOR ART

FIG. 5B



PRIOR ART

FIG. 5C



PRIOR ART